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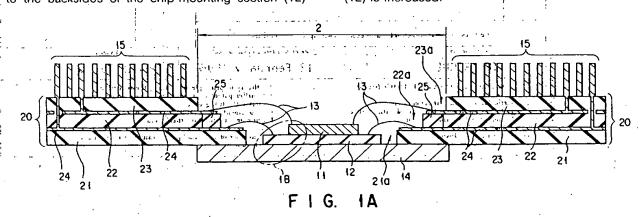
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- Semiconductor device having semiconductor chip with backside electrode.

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57) A semiconductor chip (11) is mounted on a chipmounting section (12). A conduction path forming section (20) having a plurality of conduction paths (24) formed therein is placed around the chip-mounting section (12). A heat sinking board (14) is bonded to the backsides of the chip-mounting section (12) and the conduction path forming section (20). In the conduction path forming section (20), a second insulating layer (22) is formed with notches (25), whereby the exposed area of conduction paths (24) that are wire-bonded to the chip-mounting section (12) is increased.



. The present invention relates to a semiconductor device and more particularly to a semiconductor device in which an electrode, is drawn out of the backside of an on-board semiconductor chip.

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As a form of package used for semiconductor integrated circuits there is a PGA (pin grid array). The PGA is arranged such that external terminals or pins are fixed to a package body at regular intervals, vertically and in the form of grid. The PGA is often used as a multi-terminal package. ...

 Semiconductor devices used in high frequency bands each have an electrode formed on the entire backside of their respective semiconductor chip in ; order, to stabilize their poperating characteristics. Hereinafter, such an electrode is referred to as a backside electrode. 5 5 36

. . - t... FIG. 6 shows a conventional, semiconductor ::device, having a PGA, structure... In FIG., 6, the rsemiconductor, device comprises, a semiconductor chip 101, a chip-mounting section 102, a conducting path forming section 110, a plurality of bonding wires 103, a heat sinking board 104, and a plurality , is of pin-like external terminals 112. The semiconducis envitor chip, 101 has an electrode formed on its, backside. The semiconductor chip 101 is mounted on the chip-mounting section 102. The conducting path forming section is disposed around the edges of the chip-mounting section 102 and have a plurality of conducting paths 1111 formed inside. The abonding wires 103, connect pad electrodes (not shown) formed on the semiconductor chip 101 and the chip-mounting section 102 to corresponding respective ones of the conduction paths 111. The heat sink 104 is bonded to the backside of each of the chip-mounting section 102 and the conductivepath forming section 1:10. The chip-mounting section 102 is made of an insulating material and coated on top with a conductive film not shown. The external terminals 112 are provided on the top of the conducting path, forming, section 1.1.0 and electrically connected to the respective ones of the conduction paths 14th and the constraints a

FIG. 7/is an enlarged-view of the semiconducattention chip of 01, the chip-mounting section (102, and the conduction path forming, section; (110), In this FIGURE, the conduction paths 1.11 are provided radially on first and second insulating layers 113 and 114. Each of pad electrodes 115 on the semiconductor chip :101 is connected to a respective one of the conduction paths 111 by a bonding wire 103. The backside electrode of the semiconductor chip 101 is electrically connected to the conductive Film 102a on the top of the chip-mounting section 11 102, which, in turn, is connected to a conduction path 111a on the first insulating layer 113 by bonding wires 103. Fac 1 has

. It is thus required that the conductive film 102a , on⊬the,chip-mounting section 102 be wire-bonded to the conduction path 111a when the semiconducan hitor, chip, 101 , is, coated underneath, with an electrode. In this case, as shown in FIG. 7, this wire bonding is performed at corners of the chip-mounting section, 102, and the conduction path forming section, 110, which offers little obstruction to wire bonding of the pad electrodes on the chip and allows the bonding area to be increased. ,,

The reliability of semiconductor devices is sig-10. nificantly, affected by wire bonding. Thus, good bonding must be effected at all connection points. In general, however, there is a tendency that, when a wire used is short, the resulting wire loop becomes low in height and, when a wire used is too long, it comes loose to form an underloop. In other words, the bonding wires must lie within an appropriate range of length. When a wire is short, it is liable, to peel off the point where it has been bonded. When a wire is too long, on the other hand, it may come in contact with another portion. For this reason, the length of the bonding wires between the conductive film 102a on the chipmounting section 102 and the conduction path 111a must be set appropriately.

25 The wire bonding is performed by the use of a capillary and hence there is a need for a space where it can move. In wire bonding for the semiconductor chip 101 and the conduction path 111a make in particular, the space where the capillary moves 30, must be fully taken into consideration because the semiconductor chip 101 or the second insulating layer, 114, of the conduction path forming section 1.10 forms a difference in level within the space for movement, of the capillary. That is, assuming the 35, shortest distance between a point of bonding on the conductive film 102a and the corner, of the semiconductor chip to be L1 and the shortest distance between a point of bonding on the conduction path 111a, and the corner of the second in-40, sulating layer 114 to be L2, these distances L1 and Mark L2 must be set to the shortest distance required for bonding over which the capillary can move. Thus, the size W. of the cavity shown in FIG. 6, or the In the inside diameter, of the conductive path forming 145 section 110, is defined by the size of the semiconthe injury ductor chip 101 and the space needed for wire bonding at the corners.

and FIG. 8 shows cavity size versus semiconductor : ... chip size. When no wire bonding is performed on 50 ... the chip-mounting section 102 and the conduction path forming section 110, the semiconductor chip size is allowed to lie, in the range defined by lines Aland A2. When wire bonding is performed, on the other hand, the chip size must lie within the ss., range, defined by lines, A1, and A3. To be specific, assume that the cavity size is 10 mm. If, in this case, no wire bonding is performed, the semiconductorschip size can range from 4.0 to 7.0 mm.

When wire bonding is performed, the chip size must range from 4:0 to 5.0 mm. That is, when the chip-mounting section 102 and the conduction path forming section 110 need to be connected with each other by wire bonding, the chip size is restricted within narrow limits, decreasing the versatility of the conduction path forming section (cavity) 110 or the semiconductor chip 101.

As described above, since the chip-mounting section 102 and the conduction path forming section 110 are wire bonded so as to connect the backside electrode of the semiconductor chip and the conduction path forming section 110 with each other, a space must be reserved for wire bonding. This restricts the size of a semiconductor chip.

It is an object of the present invention to provide a PGA-structured semiconductor device which has an on-board semiconductor chip with a backside electrode and permits the size of the semiconductor chip to be increased.

According to a first aspect of the present invention, there is provided a semiconductor device comprising: He of the Comprising:

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a semiconductor chip having a plurality of pad electrodes on its top and a backside electrode on ri-d a. of their staffer its backside:

a chip-mounting section on which the semiconductor chip is mounted, the chip-mounting section "having a conductive layer on its top which is in contact with the backside electrode of the semiconductor chip: 10 to 10 to

"a conduction" path forming section disposed around the chip-mounting section, the conduction bath forming section including first, second and third insulating layers, the second insulating layer being located over the first insulating layer, the third insulating layer being located over the second insulating layer, the first, second and third insulating layers having their respective openings which increase in diameter in the order of the first, second and third insulating layers, the semiconductor chip being placed in the opening of the first insulating layer; a plurality of external terminals arranged on the third insulating layer; a first group of conduction paths formed on the first insulating layers "and having their one ends exposed in the opening of the second insulating layer and their other ends "cornected to the external terminals; and a second group of conduction paths formed on the second insulating layer and having their one ends exposed in the opening of the third insulating layer and their other ends connected to the external terminals;

a first group of bonding wires for electrically ""Connecting the bne ends of the first group of conduction paths with the conductive layer of the chipmounting section; * Programme Attacks and

a second group of bonding wires for electrically 'connecting the' one ends of the second

'group of conduction paths with the pad electrodes of the semiconductor chip; and

"a heat sinking board bonded to the backside of the chip-mounting section and part of the backside of the conduction path forming section,

the second insulating layer having notches which are cut in the opposite direction to the semiconductor chip, and the exposed area of the first group of conduction paths being set larger than that of the second group of conduction paths:

"According to a second aspect of the present invention, there is provided a semiconductor device 'l'comprising: " اراكا وواد ٠.,

2 a semiconductor chip having a plurality of pad electrodes on its top and a backside electrode on do 1 do 51 08 its backside;

113.0 a conduction path forming section disposed around the semiconductor chip, the conduction path forming section including first, second and 20 th third insulating layers; the second insulating layer Cambin being located over the first linsulating layer, the villa "third insulating layer being located over the second "I findulating layer, the first, second and third insulatwhich ind layers having their respective openings which 25 increase in diameter in the order of the first, second and third insulating layers, the semiconductor chip being placed in the opening of the first insulating layer a plurality of external terminals arranged of the third insulating layer, a first group of conduction paths formed on the first insulating layers and having their one ends exposed in the opening of the second insulating layer and their other ends connected "to" the external terminals; a second 13 flogroup of conduction paths formed on the second insulating layer and having their one ends exposed " In the opening of the third insulating layer and their other ends connected to the external terminals; and was a conductor formed in the first insulating layer and Thaving its one end connected to the first group of do conduction paths and its other end exposed on the backside of the first insulating layer; har to

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a chip-mounting section provided on the back-20.00 side of the first insulating layer and coated on top with a conduction dayer on which the semiconduc-"tor chip is mounted, the backside electrode of the semiconductor chip and the other end of the conductor in the first insulating layer being connected together by the conduction layer; Additions

bonding lwires, for electrically connecting the one ends of the second group of conduction paths with the pad electrodes of the semiconductor chip; and to the same than 1.1:

a heat sinking board bonded to backsides of the chip-mounting section and the first insulating Layer Control of Figure 1 1 1 1 11 11 1

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in

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· which:

FIG. 1A is a diagrammatic sectional view of a semiconductor device according to a first embodiment of the present invention;

FIG. 1B is an enlarged view of a portion indicated by circle 1B in FIG. 1A;

FIG. 2 is a plan view of a portion corresponding to line 2 in FIG. 1A;

FIG. 3 is an enlarged perspective view of a portion indicated by circle 3 in FIG. 2;

FIG. 4A is a diagrammatic sectional view of a semiconductor, device according to a second embodiment of the present invention;

FIG. 4B is fant enlarged view of a portion indicated by circle 4B in FIG. 4A; here per FIG. 15A is a diagrammatic sectional view of a semiconductor device according to a third embodiment of the present invention;

FIG. 5B is an enlarged view of a portion indicated by circle 5B in FIG. 5A; street in the street of a street of

FIG. 17 is an enlarged sectional view of a portion of the semiconductor device of FIG. 6; and,

tween the semiconductor chip size and the cav-

FIGS. 1A and 1B show a semiconductor device according to a first embodiment of the present invention. The semiconductor device comprises a semiconductor chip 11, a chip-mounting-section 12) a conduction path forming section 20, bonding wires 43, a heat sinking board 14; and pin-like external terminals 15. The semiconductor chip 11 is mounted on the chip-mounting section 12. The conduction; path, forming section; 20, is disposed around the chip-mounting section, 12 and has a and the plurality of conduction paths 24 formed inside. The bonding (wires), 13 electrically, connect pad electrodes (not shown) on the semiconductor chip 11 and the chip-mounting section 12 with the conduc-. ... tion paths .24. The heat sink .14 is bonded to the backsides of the chip-mounting section 12 and the the conduction path forming section; 20. The external • • terminals 15 are provided on the top of the conducpertion path forming section 20; in a per apprecia-

The conduction path forming section 20, comprises a first insulating layer 21, a second insulating layer 22, a third insulating layer 23, and conduction paths 24 interposed between every insulating layer. The first, second and third insulating layers 21, 22 and 23 respectively have square openings 21a, 22a and 23a each having a different diameter. Of these openings, the uppermost opening 23a is the greatest in diameter, followed by the opening:22a. Thus, the insulating layers 21, 22 and 23 form steps at their central portion. The second insulating layer 22 has notches 25 formed at the

the four corners of the square opening 22a. The immotches will be described later in detail. Each of the conduction paths has its end exposed at the opening and its other end electrically connected to

a corresponding one of the external terminals 15.

FIG. 1B is an enlarged view of a portion indicated by circle 1B in FIG. 1A. The semiconductor chip. 1.1 has a backside electrode 11a produced by metal evaporation onto its backside. The chipmounting section 12 consists of a highly insulating material and is coated on top with a metal layer 121. The backside of the semiconductor chip. 11 is bonded to the metal layer 121 by a conductive adhesive 16. The heat sink 14 is bonded to the backside of the chipmounting section 12 by an adhesive 17. This adhesive 17 may be either insulating or conducting. The heat sink 14 is also bonded to the backside of the conduction path forming section 20 by the adhesive 17.

to line 2 in Fig. 1A with bonding wires 13 omitted on the left side of a diagonal dashed and dotted line. As can be seen from this figure, the conduction paths 24 extend radially on the first and second insulating layers 21 and 22. The second insulating layer 22 is formed at its respective corners with notches 25. Each notch is formed in the opposite direction to a corresponding one of the corners of the semiconductor chip 11.

30 yil with The notches 25 will be further described with reference to FIG. 3. The notches 25 are formed at but the corners of the second insulating layer 22. Each notch increases the exposed area of the conduction, path 24a formed on the first insulating layer 35% D21% One of the bonding wires 13 has its one end vir bonded to the metal layer 121 and its other end bonded to that portion of the conduction path 24a multiplication is exposed by the notch 25. This permits the bonding wire 13 to be set to an appropriate length. 40 tus Moreover, the point of bonding on the chip-mount-; ing section 12 can be put away from the semiconand inductor chip 11, permitting the distance L1, to be set Is a long. Thus, the metal layer 121 and the conduction can path, 24a can be readily connected to each other 45i., by: wires, In, addition, the distance L2, can also be 11 ; set slong, which permits a sufficient space to be greserved for movement of the capillary. Furthermore, since the notches 25 are formed at the corners of the second insulating layer 22, the pad 50 electrodes; 27, on the semiconductor chip 11 and the conduction paths 24 on the second insulating and layer 22 can be connected together by bonding the two wires:13 in the same manner as the prior art,

Here, L1 is the shortest distance between the point of bonding on the chip-mounting section 12 and the semiconductor chip 11, and L2 is the distance, between the point of bonding on the conduction path 24a and the intersection of a straight



line along the bonding wire and the second insulating layer 22, i.e., the distance between the point of bonding on the conduction path 24a and the deepest point in the notch 25.

According to the first embodiment of the present invention, the notches 25 are provided at the corners of the square opening 22 in the second insulating layer 22 to thereby increase the exposed area of the conduction path 24a that is wire-bonded to the chip-mounting section 12. Thus, the space for movement of the capillary can be increased, thereby permitting easy bonding. In addition, the bonding wires can be set to an appropriate length, which prevents the wires from peeling off.

Since the exposed area of the conduction path 24a is increased, the points of bonding on the chipmounting section 12 can be put away from the semiconductor chip even if the length of the bonding wires is set appropriately. For this reason,

In the first embodiment, the notches 25 are provided at the corners of the second insulating layer 22. This is not restrictive. The notches may be provided at other portions of the second insulating layer than its corners if they are located over the conduction paths 24a. In other words, the conduction paths 24a can be located in any position on the first insulating layer 21 where they do not come into contact with other bonding wires, and the notches 25 can be formed on such conduction paths:

Next, reférence will be made to FIGS. 4A and 4B to describe à second embodiment of the present invention. In FIGS. 4A and 4B like reference numerals are used to denote corresponding portions to those in the first embodiment, and only different portions will be described below.

ted on the chip-mounting section 12 by means of a conductive adhesive (not shown). The first insulating layer 21 is undercut along its opening 21a to form an undercut portion 26. The periphery of the chip-mounting section 12 is fit into the undercut 26 of the insulating layer 21. The backsides of the chip-mounting section 12 and the conduction path forming section 20 are bonded to the heat sink 14 by means of an insulating adhesive (not shown).

FIG. 4B is an enlarged view of a portion indicated by circle 4B in FIG. 4A. In FIG. 4B, the first insulating layer 21 is formed with a conduction path 24b which passes through that layer and is connected with the conduction path 24b on the first insulating layer 21. The metal layer 121 provided on the top of the chip-mounting section 12 and the conduction path 24b are electrically connected with each other by means of conductive adhesive 16. That is, the backside electrode of the semiconductor chip 11 is electrically connected to the conduction of the conduction of the semiconductor chip 11 is electrically connected to the conduction of the semiconductor chip 11 is electrically connected to the conduction of the semiconductor chip 11 is electrically connected to the conduction of the semiconductor chip 11 is electrically connected to the conduction of the semiconductor chip 11 is electrically connected to the conduction of the semiconductor chip 11 is electrically connected to the conduction of the conduction of the chip 11 is electrically connected to the conduction of the chip 11 is electrically connected to the conduction of the chip 11 is electrically connected to the conduction of the chip 11 is electrically connected to the conduction of the chip 11 is electrically connected to the conduction of the chip 11 is electrically connected to the conduction of the chip 11 is electrically connected to the chip 11 is electrically connected to the chip 11 is electrically chip 12 is electrically chip 12 is electrically chip 12 is electrically chip 13 is electrically chip 13 is electrically chip 14 is electrically chip 15 is electrically ch

tion path 24a through the metal layer 121, conductive adhesive 16 and conduction path 24b without using wire bonding.

It is needless to say that the pad electrodes (not shown in FIGS. 4All and 4B) on the semiconductor chip 11 are connected by bonding wires to the conduction paths radially arranged on the first insulating layer 21 or second insulating layer 22.

Next, a third embodiment of the present invention will be described with reference to FIGS. 5A and 5B. Like reference numerals are used to democrate corresponding parts to those in the second embodiment. The present embodiment uses an insulating heat sinking board 30, which serves as a chip-mounting section and a heat sink. A metal layer 121 is deposited onto the top of the insulating heat sinking board 30, and the semiconductor chip 11 is bonded to the metal layer 121 by a conductive adhesive not shown.

FIG. 5B its an enlarged view of as portion indicated by circle 5B in FIG: 5A. The insulating heat sinking board 30 has a stepped portion 31 along its periphery. The stepped portion 31 of the heat sinking board 30 is fit into the undercut portion 26 of the first insulating layer 21 and they are bonded to each other by a conductive adhesive 49. The backside electrode (not shown) of the semiconductor chip 141 is electrically connected to the conduction path 24a through the conductive adhesive 16, met-

In the second embodiment, the conduction unit-reath forming section 20 and the chip mounting section 12 are electrically connected together by 35 the conductive adhesive 16, and, in the third embodiment, the conduction path forming section 20 · # and the insulating heat sinking board 30 are elecand trically connected together by the conductive adhe-The sive 19. That is, the second and third embodiments 40' Heliminate the need for the metal-layer 121 and the for conduction path 24a to be wire-bonded together as and in the first embodiments Thus, there is no restric-** Otion on semiconductor chip size. Namely, the chip tantalsize can be increased). The use of a semiconductor 45 Chip about the size of a cavity is allowed. Also, the semiconductor chip size can be made substantially the other same as when no electrode is drawn out of the But backside of the chip. The Date of the Artist of the Ar

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1. A semiconductor device characterized by com-

a chip-mounting section (12) on which said semiconductors chip is mounted, said, chip-

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mounting section having a conductive layer (121) on its top which is in contact with said backside electrode of said semiconductor chip;

a conduction path forming section (20) disposed around said chip-mounting section (12), said conduction path forming section including first, second and third insulating layers (21, 22, 23), said second insulating layer (22) being located over said first insulating layer (21), said third insulating layer .(23) being located over said second insulating layer, said first, second and third insulating layers having their respective openings (21a, 22a, 23a) which increase in diameter in the order of said first, second and third insulating layers, said semiconductor chip (11) being placed in said opening of said first insulating layer (21); a plurality of external terminals (15) arranged on said third insulating layer (23); a first group of conduction paths (24) formed on said first insulating layer (21) and having their one ends exposed in said opening of said second insulating layer (22) and their other ends connected to said external terminals (15); and a second group of conduction paths (24) formed on said second insulating layer (22) and having their one ends exposed in said opening of said third insulating layer (23) and their other ends connected to said external terminals (15);

a first group of bonding wires (13) for electrically connecting said one ends of said first group of conduction paths (24) with said conductive layer (121) of said chip-mounting section (12);

a second group of bonding wires (13) for electrically connecting said one ends of said second group of conduction paths (24) withsaid pad electrodes (115) of said semiconductor chip (11); and

a heat sinking board (14) bonded to said backside of said chip-mounting section (12) and part of the backside of said conduction path forming section (20),

said second insulating layer (22) having notches (25) which are cut in the opposite direction to said semiconductor chip (11), and the exposed area of said first group of conduction paths (24) being set larger than that of said second group of conduction paths (24).

A device according to claim 1, characterized in that each of said openings (21a, 22a, 23a) of said first, second and third insulating layers is square, and said notches (25) are formed at corners of said opening of said second insulating layer (22).

1..., 3.1 A, device according to claim 1, characterized in that said first group of bonding wires (13) have their one ends bonded to those parts of said where first group, of conduction paths (24a) which are 5-to conserve exposed in said notches (25) and their other particle ends bonded to said conduction layer (121) of \dots 4. y _qsaid, chip-mounting section (12).

1 19 185 DEC 1 4. A semiconductor device characterized by com-

, a semiconductor chip (1.1) having a pluraland a like ity, of pad electrodes (115) on its top and a backside electrode (11a) on its backside;

a conduction path forming section (20) disposed around said semiconductor chip, said conduction path forming section (20) including first, second and third insulating layers (21, 22, 23), said second insulating layer (22) being located over said first insulating layer (21), said third insulating layer (23) being located over said second insulating layer (22), said first, second, and, third insulating layers, having their respective openings (21a, 22a, 23a) which increase in diameter in the order of said first, second and third insulating layers, said semiconductor chip (11) being placed in said open-. ing of said first insulating layer; a plurality of external terminals (15) arranged on said third insulating layer (23); a first group of conduction paths (24) formed on said first insulating layer (21) and having their one ends exposed in said opening of said second insulating layer (22) and their other ends connected to said external terminals (15); a second group of conduction paths (24) formed on said second insulating layer (22) and having their one ends exposed in said opening of said third insulating layer (23) and their other ends connected to said. external terminals (15); and a conductor (24b) formed in said first insulating layer (21) and having its one end connected to said second group of conduction paths (24) and its other end exposed on the backside of said first insulating layer (21);

a chip-mounting section (12) provided on the backside of said first insulating layer (21) and coated on top with a conductive layer (121) on which said semiconductor chip (11) is mounted, said backside electrode (11a) of said semiconductor chip (11) and the other end of said conductor (24b) in said first insulating layer being connected together by said conductive layer (121);

bonding wires (13) for electrically connecting said one ends of said second group of conduction paths (24) with said pad electrodes (115) of said semiconductor chip (11); and

a heat sinking board (14) bonded to back-

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sides of said chip-mounting section (12) and said first insulating layer (21).

5. 'A device according to claim 4, characterized in that said first insulating layer (21) has an undercut portion (26) formed along its opening, and the other end of said conductor (24a) in said first insulating layer is exposed in said undercut portion.

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- 6. A device according to claim 5, characterized in that the periphery of said chip-mounting section (12) is fit into said undercut portion (26) of said first insulating layer (21), and the other end of said conductor (24a) is in contact with said conductive layer (121) of said chip-mounting section at said undercut portion.
- 7. A device according to claim 4, characterized in that said chip-mounting section (12) and said heat sinking board (14) have insulating and heat sinking properties and are formed integral with each other.

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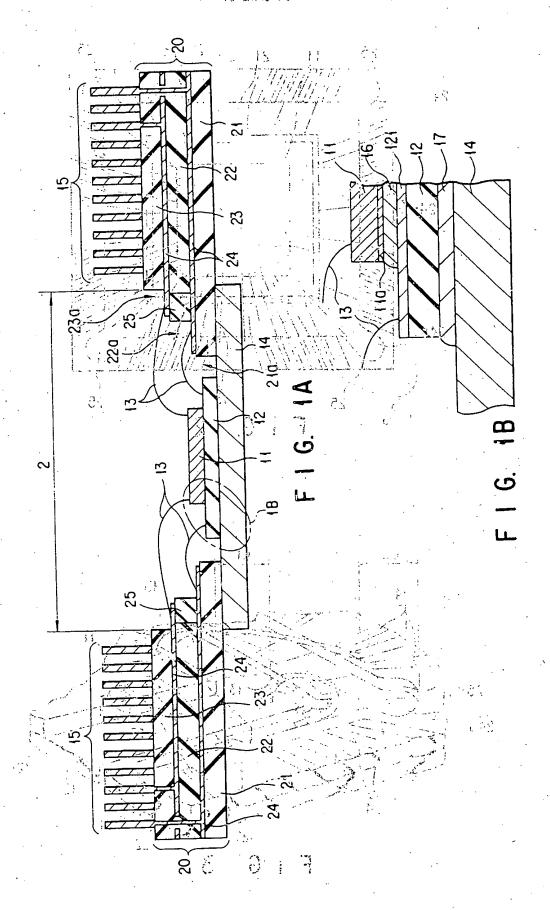
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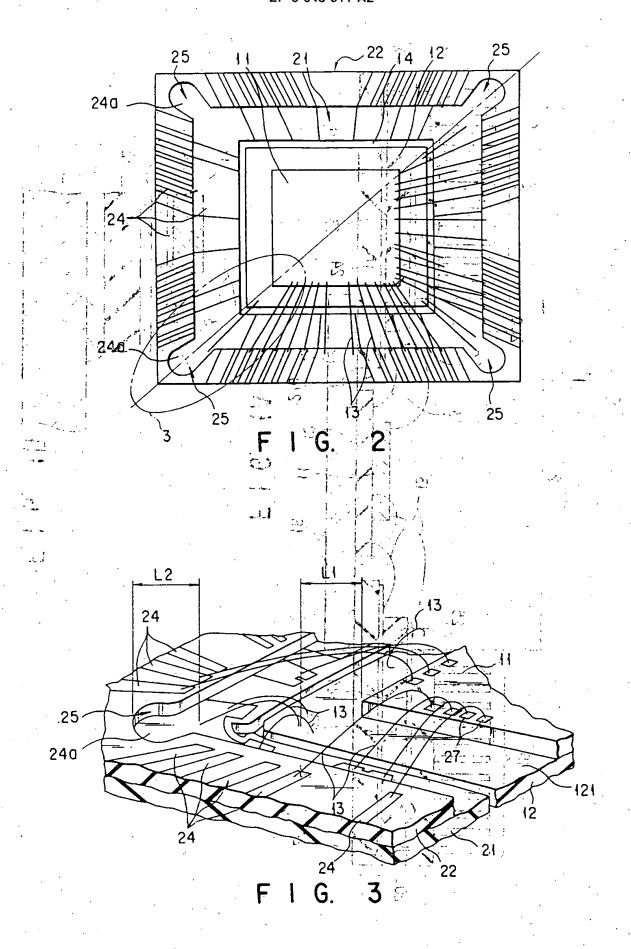
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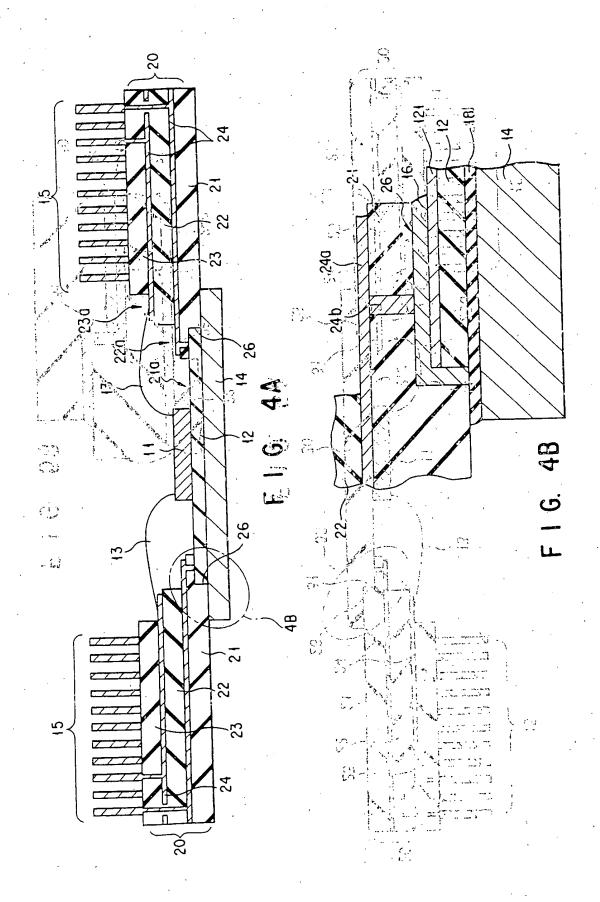
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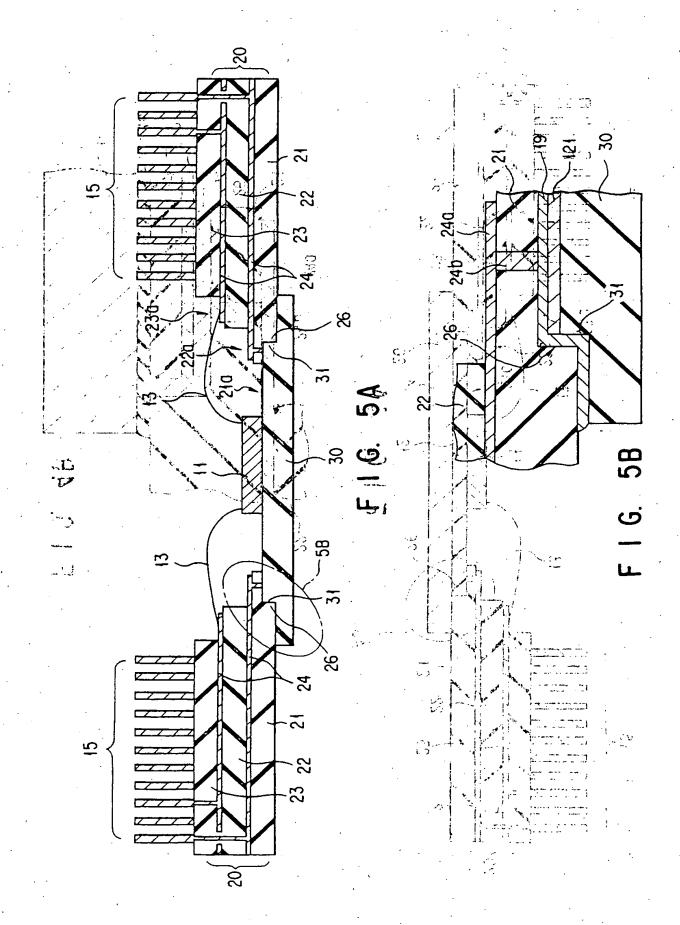
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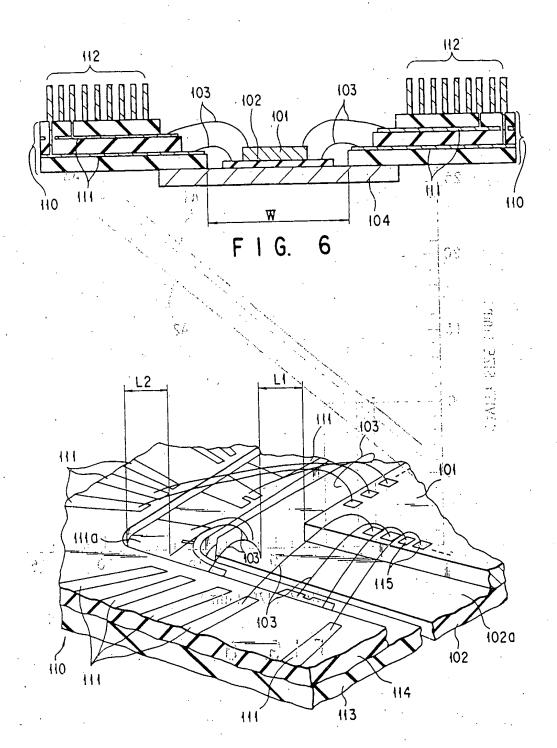
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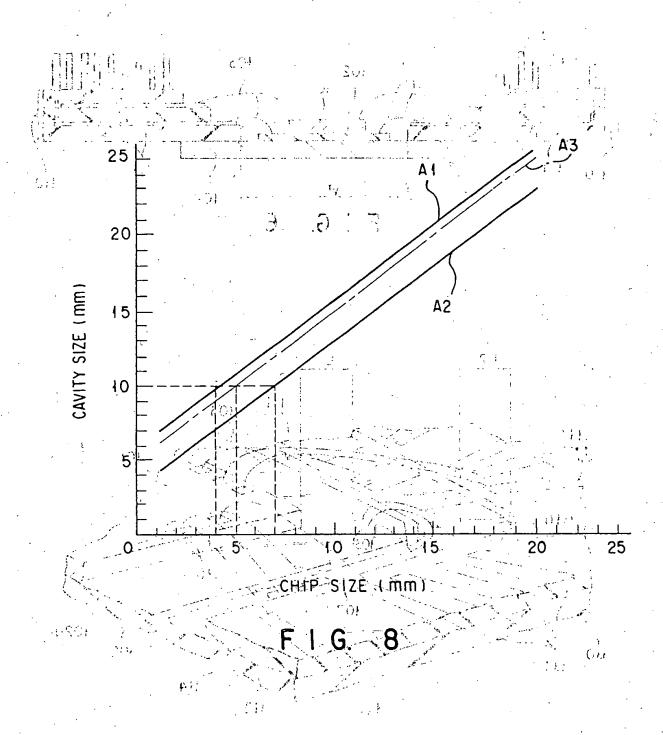








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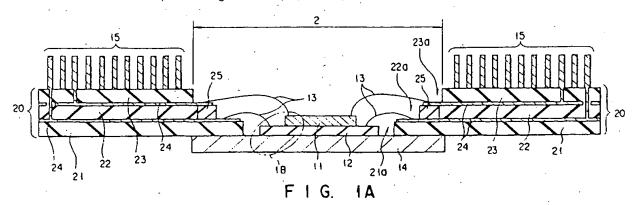
Date of deferred publication of the search report: 20.09.95 Bulletin 95/38 Applicant: KABUSHIKI KAISHA TOSHIBA 72, Horikawa-cho, Saiwai-ku Kawasaki-shi, Kanagawa-ken 210, Tokyo (JP)

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Semiconductor device having semiconductor chip with backside electrode.

(57) A semiconductor chip (11) is mounted on a chipmounting section (12). A conduction path forming section (20) having a plurality of conduction paths (24) formed therein is placed around the chip-mounting section (12). A heat sinking board (14) is bonded to the backsides of the chip-mounting section (12) and the conduction path forming section (20). In the conduction path forming section (20), a second insulating layer (22) is formed with notches (25), whereby the exposed area of conduction paths (24) that are wire-bonded to the chip-mounting section (12) is increased.



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EUROPEAN SEARCH REPORT 5 9 80 13

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Application Number

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-	The present search report	has been drawn up for all claims			
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X: Y:	CATEGORY OF CITED DO: particularly relevant if taken alon particularly relevant if combined	E : earlier : after : D : docum	r or principle underlyin r patent document, but the filing date nent cited in the applic tent cited for other rea	ation	